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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/733,402	12/08/2000	Stephen R. Vogel	DIVA /203	1879

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EXAMINER	
RAMPURIA, SATISH	
ART UNIT	**PAPER NUMBER**
2124	7

DATE MAILED: 02/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/733,402	VOGEL ET AL.	
	Examiner	Art Unit	
	Satish S. Rampuria	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the application filed on December 8, 2000.

2. Claims 1-54 are pending.

Information Disclosure Statement

3. An initialed and dated copy of Applicant's IDS form 1449, Paper No. 02, is attached to the instant Office action.

Drawings

4. The drawings are objected to because the first figure is not numbered. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-11, 13-29, 31-39, 41-43, and 45-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herrmann et al., hereinafter called Herrmann, US Patent No. 6,134,707 and further in view of Tang, US Patent No. 6,389,321.

As per claims 1, 3, 6, 8, 9, 10, 27, 34, 36, 38, 42, 43 and 45 Herrmann discloses:

- a first file including programmable logic instructions in a non-native format (Abstract, "a device configuration program with adaptive programming source code instructions (non-native format) that characterize device (programmable) configuration instructions and data")

- converting said non-native format programmable logic instructions into programmable logic instructions having a format native to said remote programmable logic device (Abstract, "An interpreter converts the device configuration program into formatted device (programmable) configuration instructions and data"). It is interpreted that file is being converted it must be stored in a format which processor understand, and processor is included inherently.

- a second file including said native format programmable logic instructions (Abstract, "The formatted device configuration instructions and data (native format) are used to program a programmable device in the manner specified by the adaptive programming source code instructions")

- programming said selectively accessed programmable logic devices via a JTAG bus (col. 4, lines 56-60 "The PCB... includes... embedded controller 34... JTAG interface circuitry... A bus... route... programming signals... to the IC").

Hermann did not explicitly disclose receiving/transmitting file via communication medium, executing the converted file to a device via a bus, and programming a device via a bus.

However, Tang in analogous system for programming a PLD discloses receiving/transmitting file via communication medium, executing the converted file to a device via a bus, and programming a device via a bus (col. 1, lines 42-43 "sending and receiving data (file) over a communication link" and col. 5, lines 61-65 "The microprocessor, which executes a program stored in the non-volatile memory (e.g., EPROM 608), specifies an address on an address bus (e.g., address bus 604), so as to store the data on the data bus into memory (e.g., RAM 607)" and col. 4, lines 49-50 "The programming data stored in RAM 607 can be provided to ISP controller 402 via data bus").

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to program PLD via communication medium, execute file, and program PLD via a bus as taught by Tang in corresponding to program PLD as taught by Herrmann. The modification would be obvious because of one of ordinary skill in the art would be motivated to program PLD remotely including execution and programming a PLD as suggested by Tang (col. 1, lines, 25-33).

As per claims 2, 7, 31, 37, and 39 the rejection of claims 1 and 6 respectively, is incorporated and further Tang discloses:

- ***wherein said first communications medium comprises an Ethernet network*** (col. 2, lines 13-15 "host units... coupled by a computer network... a local area network or a wide area network")

Claims 13 and 19 are the apparatus claim corresponding to method claim 1 and rejected under the same reason set forth in connection of the rejection of claim 1 above. It is interpreted for the data to be converted the converter program must be stored in.

Claim 14, 21 is the apparatus claim corresponding to method claim 2 and rejected under the same reason set forth in connection of the rejection of claim 2 above.

Claim 15 is the apparatus claim corresponding to method claim 3 and rejected under the same reason set forth in connection of the rejection of claim 3 above.

Claim 26 is the product claim corresponding to method claim 1 and rejected under the same reason set forth in connection of the rejection of claim 1 above.

As per claims 5, 35, and 46 the rejection of claims 1, 27, and 36 is incorporated respectively, and further it is interpreted that after programming is done the device must enter in initial operating state to function properly and to make the new changes in effect.

As per claims 4, 11, 32, and 41 the rejection of claims 1, 6, 27, and 36 is incorporated respectively, and further the system disclosed by Herrmann and modified by Tang's teaching in the manner set forth above would include a JTAG format.

- ***wherein said native format comprises a JTAG format*** (Abstract, "formatted device configuration instructions and data are preferably compatible with IEEE 1149.1 JTAG-BST specifications")

Claims 16, 23 are the apparatus claim corresponding to method claim 4 and rejected under the same reason set forth in connection of the rejection of claim 4 above.

Claims 17, 18 are the apparatus claim corresponding to method claims 8 and 9 respectively and rejected under the same reason set forth in connection of the rejection of claims 8 and 9 respectively above.

Claim 22 is the apparatus claim corresponding to method claim 3 and rejected under the same reason set forth in connection of the rejection of claim 3 above.

Claim 24 is the apparatus claim corresponding to method claim 8 and rejected under the same reason set forth in connection of the rejection of claim 8 above.

Claim 25 is the apparatus claim corresponding to method claim 9 and rejected under the same reason set forth in connection of the rejection of claim 9 above.

As per claims 20 and 28, the rejection of claims 19 and 27 is incorporated and further Herrmann discloses:

- ***wherein said first file is a POF file*** (col. 2, lines 22-24 "a programming object file (POF) is loaded onto the computer running the programming software")

As per claim 29, the rejection of claim 27 is incorporated and further Tang discloses:

- ***wherein said remote programmer source is selected from the group comprising a workstation, and a personal computer*** (col. 2, lines 10-13 "Each host computer includes a central processing unit, which may be a personal computer or an engineering workstation, and an access interface for accessing the communication link")

As per claim 33, the rejection of claim 27 is incorporated and further Tang discloses:

- ***wherein said first bus is a board select bus*** (col. 5, lines 12-16 "The data processing... include... sub-system functional components: a processor 64, memory 66, input/output circuitry 68, and peripheral devices 70. These components are coupled together by a system bus 72")

7. Claims 12, 44, 47-50, and 52- 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hermann, Tang and further in view of Sasaki, hereinafter called Sasaki, US Patent No. 6,198,304.

As per claims 12 and 47, the rejection of claims 6 and 46 is incorporated respectively, and further neither Tang nor Herrmann discloses resetting the programmable logic device.

However, Sasaki discloses resetting programmable logic device (col. 12, lines "power to the PLD... is turned off or a reset signal is applied... PLD being programmed, such as PLDs... pin indicates... programming... completed... commencement of normal operation begins.").

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to resetting the method of programmable logic device as taught by Hermann and Tang using the teaching of Sasaki. The modification would be obvious because of one of ordinary skill in the art would be motivated to reset the device to make the new changes effective.

As per claims 44, 48, and 54 Herrmann discloses:

- a processor system coupled to said at least one switching circuit via a board select bus and a JTAG bus (col. 4, lines 56-60 "The PCB... includes... embedded controller 34... JTAG interface circuitry... A bus... route... programming signals... to the IC").

Hermann did not explicitly disclose executing a file in a format native to PLD.

However, Tang in analogous system for programming a PLD discloses executing of a file for a device e.g. EEPROM (col. 5, lines 61-65 "The microprocessor, which executes a program stored in the non-volatile memory (e.g., EPROM 608)").

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the executing of a file by a processor for a device as taught by Tang in corresponding to program PLD using JTAG bus as taught by Hermann. The modification would be obvious because of one of ordinary skill in the art would be motivated to execute a file format native to PLD to program the PLD.

Neither Herrmann nor Tang discloses system using switching circuit.

However, Sasaki's system discloses using switching circuit to program PLD (col. 21, lines 47-50 "random access memory includes two arrays of memory storage elements and a switching circuit connected to both of said two arrays of memory storage elements and said input node")

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to include switching circuit to program PLD as taught by Sasaki in corresponding to the program PLD as taught by Herrmann. The modification would be obvious

because of one of ordinary skill in the art would be motivated to include switching circuit to control the data in the system to program PLD.

As per claim 49, the rejection of claim 48 is incorporated and further Herrmann nor discloses:

- ***wherein said first and second bus is a backplane*** (col. 4, lines 49-56 "The programming data stored... provided... via data bus...under... microprocessor ... provides a control signal... for latching... data into ISP controller 402. In this manner, the multiple ISP controllers in ISP system 600 can program a large number of ISP devices in parallel, without incurring large latencies due to the long daisy-chains of ISP devices")

As per claim 50, the rejection of claim 48 is incorporated and further the system disclosed by Herrmann and modified by Tang's teaching in the manner set forth above would include a JTAG format.

- ***wherein said native format comprises a JTAG format*** (Abstract, "formatted device configuration instructions and data are preferably compatible with IEEE 1149.1 JTAG-BST specifications")

As per claim 52, the rejection of claim 48 is incorporated, and it is interpreted that programmable logic device is selected from field programmable gate array as admitted prior art (page 1, lines 12-13 "programmable logic devices (PLDs), such field programmable gate array (FPGAs and the like, are well known")

As per claim 53, the rejection of claim 48 is incorporated and further Tang discloses:

- ***wherein processor system is a server*** (col. 2, lines 59-61 "the ISP system is programmed by remote access by a host programming system which includes one or more programming host computers")

8. Claims 30, 40, and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tang, in view of technical paper from Altera Corporation published in May 1999, ver. 6, hereinafter called Altera Corporation.

As per claims 30 and 40 the rejection of claims 27 and 36 is incorporated respectively, and Tang does not explicitly disclose using a JAM byte code file.

However, Altera Corporation discloses using the JAM byte code file the time of programming PLD (page 7, paragraph 1 "The Jam language allow a sing Jam file (.jam) or Jam Byte-Code file (.jbc) to contain both the data to be programmed into a device and the algorithm required to accomplish programming).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the JAM byte code file to program PLDs as taught by Altera Corporation in the programming and remotely programming PLDs as taught by Herrmann and Tang. The modification would be obvious because of one of ordinary skill in the art would be motivated to include the JAM byte code file to reduce the time, file size and large algorithms in system programming as suggested by Altera Corporation (page 6, paragraph 3 "The Jam™ programming... in-system programming").

Claim 51 is the apparatus claim corresponding to method claims 30 and 40 respectively, and the rejection of claim 48 is incorporated and rejected under the same reason set forth in connection of the rejection of claims 33 and 40 respectively, above.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patent is cited to further show the state of the art with respect to programming the programmable logic device.

US Patent No. 5,635,855 to Tang

US Patent No. 5,338,982 to Kawana

US Patent No. 5,237,218 to Josephson et al.

The following patent is cited to further show the state of the art with respect to remotely upgrading / distributing.

US Patent No. 6,535,911 to Miller et al.

US Patent No. 6,578,198 to Freeman et al.

US Patent No. 6,675,201 to Parkkinen

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Satish Rampuria whose telephone number is 703-305-8891.

The examiner can normally be reached on Monday-Friday from 8:30 A. M. to 5:00 P.M. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Kakali Chaki can be reached at 703-305-9662. The fax number for this group is 703-872-9306. An inquiry of general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is 703-305-3900.

Satish S. Rampuria

Patent Examiner

Art Unit 2124

02/23/04

WEI Y. ZHEN
PRIMARY PATENT EXAMINER